Floorplan for implementation methodology for the next MSoT Smart Power (BCD) designs

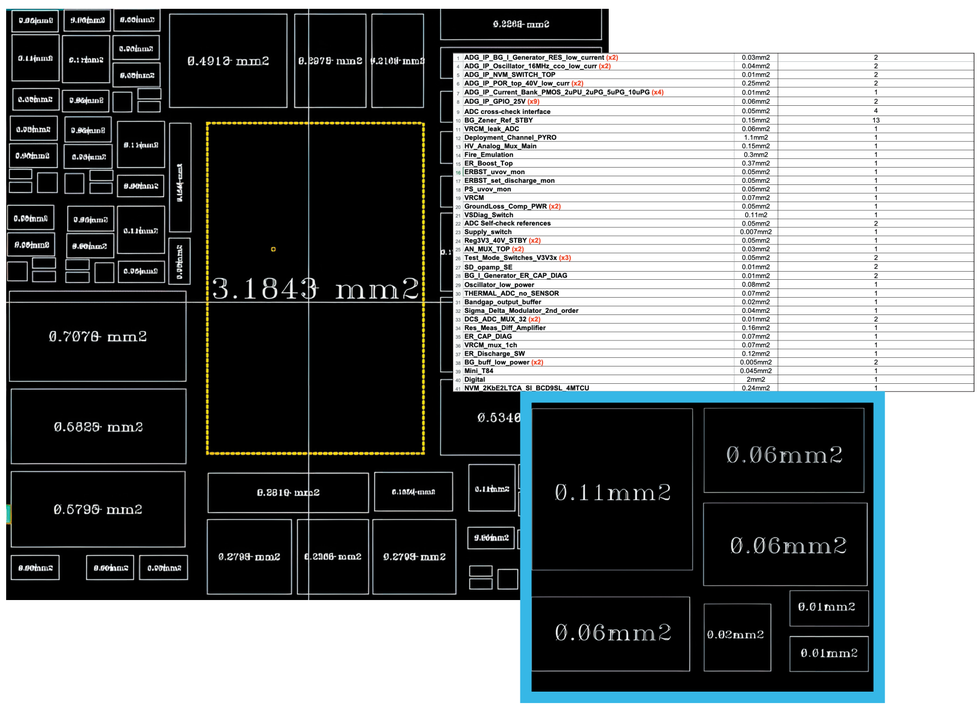
By Livio Fratantonio, Massimiliano Innocenti, Riccardo Guglielmo from STMicroelectronics | Stefano Basile, Jonhatan Olave from Cadence
Email: livio.fratantonio@st.com, Massimiliano.innocenti@st.com, Riccardo.guglielmo@st.com, stefano@cadence.com, jolave@cadence.com

1. CONTEXT AND MOTIVATION:

in today's dynamic system design scenarios, the complexity of analog mixed signal designs is increasing significantly as the technology evolves. Advanced methodologies are required to improve the quality of reliable products and globally increase the layout productivity to reduce time to market. For smart power designs, the relatively few metal levels for signal routing, aggressive voltage-dependent rules, and complex spacing tables mean that a well-designed floorplan during early stages is the key to saving design area and closing chip-level routing to avoid congestion issues for the timely release of PG tapes.

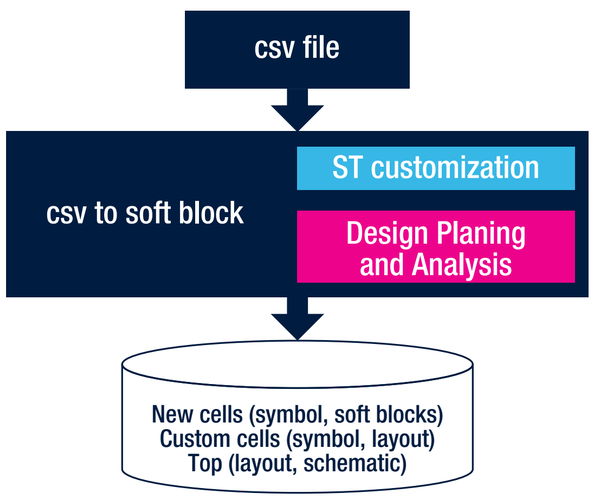
2. LAYOUT DESIGN BEGINS WITHOUT TOP IC SCHEMATIC

Old approach



ADG_IP_BG_I_Generator_RES_low_current (x2)	0.03mm2	2
ADG_IP_Oscillator_16MHz_cco_low_curr (x2)	0.04mm2	2
ADG_IP_NVM_SWITCH_TOP	0.01mm2	2
ADG_IP_POR_top_40V_low_curr (x2)	0.25mm2	2
ADG_IP_Current_Bank_PMOS_2uPU_2uPG_5uPG_10uPG (x4)	0.01mm2	1
ADG_IP_GPIO_25V (x8)	0.06mm2	2
ADC cross-check interface	0.05mm2	4
BG_Zener_Ref_STBY	0.15mm2	13
VRCM_leak_ADC	0.06mm2	1
Deployment_Channel_PYRO	1.1mm2	1
HV_Analog_Mux_Main	0.15mm2	1
Fire_Emulation	0.3mm2	1
ER_Boost_Top	0.37mm2	1
ERBST_uvov_mon	0.05mm2	1
ERBST_set_discharge_mon	0.05mm2	1
PS_uvov_mon	0.05mm2	1
VRCM	0.07mm2	1
GroundLoss_Comp_PWR (x2)	0.05mm2	1
VSDiag_Switch	0.11m2	1
ADC Self-check references	0.05mm2	2
Supply_switch	0.007mm2	1
RegSV3_40V_STBY (x2)	0.05mm2	1
AN_MUX_TOP (x2)	0.03mm2	1
Test_Mode_Switches_V3V3x (x3)	0.05mm2	2
SD_opamp_SE	0.01mm2	2
BG_I_Generator_ER_CAP_DIAG	0.01mm2	2
Oscillator_low_power	0.08mm2	1
THERMAL_ADC_no_SENSOR	0.07mm2	1
Bandgap_output_buffer	0.02mm2	1
Sigma_Delta_Modulator_2nd_order	0.04mm2	1
DCS_ADC_MUX_32 (x2)	0.01mm2	2
Res_Meas_Diff_Amplifier	0.16mm2	1
ER_CAP_DIAG	0.07mm2	1
VRCM_mux_1ch	0.07mm2	1
ER_Discharge_SW	0.12mm2	1
BG_buff_low_power (x2)	0.005mm2	2
Mini_T84	0.045mm2	1
Digital	2mm2	1
NVM_2KbE2LTCA_SI_BCD9SL_4MTCU	0.24mm2	1

New approach



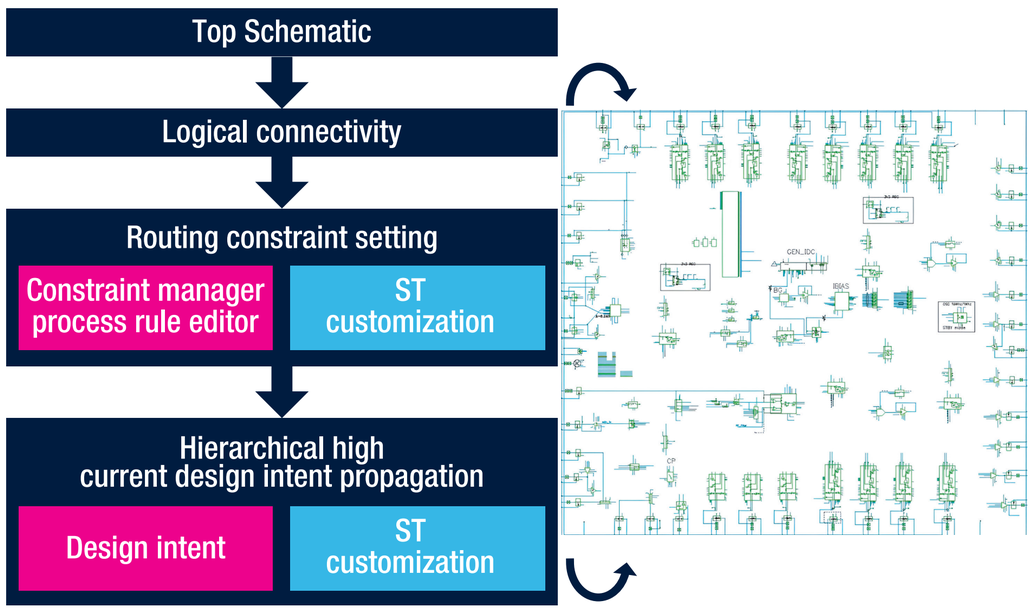
Old approach: area and occurrences (in csv file) are used to draw block shapes on the canvas.

New automatic approach based on ST customization:

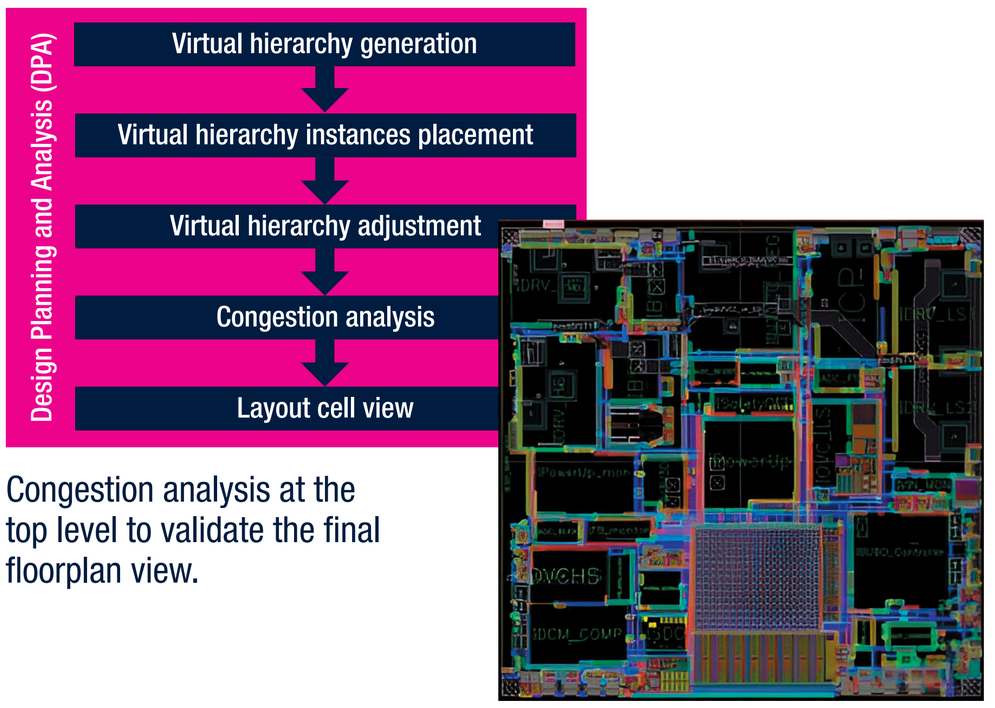
- New cells (in csv file)
  - Symbol (property area)
  - Soft block (proper area)
- Custom cells (in csv file)
  - Original symbol/layout
- Top schematic/layout generation.

3. TOP IC SCHEMATIC IS FINALIZED

Logical connectivity, design routing constraints, and high current design intent propagation.



4. TOP IC LAYOUT FLOORPLAN IS IMPLEMENTED EARLIER



Congestion analysis at the top level to validate the final floorplan view.

Conclusions

The benefits of this flow include:

- Automatic early estimation of chip area (few minutes vs days).
- "Design planning and analysis" improves floorplan view generation and prevents routing congestion issues (significant reduction in turnaround time).
- The current values stored in high current design intents enable routing to be current-aware without simulation data.
- The automotive design community has tight tapeout schedules, and this approach saves design steps to help meet time-to-market requirements.